WHAT IS CLAIMED IS:

1. An apparatus for controlling a boosted voltage, comprising:

a voltage generating circuit configured to generate a boosted voltage from an input voltage based on a control current; and

a control circuit configured to generate the control current based on the boosted voltage.

2. The apparatus of claim 1, wherein the voltage generating circuit comprises:

a capacitor; and

a switching structure configured to selectively store charges corresponding to the input voltage in the capacitor, and to selectively output the stored charges in conjunction with charges corresponding to the control current as the boosted voltage.

3. The apparatus of claim 2, wherein the control circuit is configured to generate the control current based on a difference between the boosted voltage and a desired boosted voltage.

4. The apparatus of claim 1, wherein the voltage generating circuit comprises:

first, second, third and fourth switches; and

a capacitor configured to store charges corresponding to the input voltage while the first and third switches are turned on, and outputting the boosted voltage

while the second and fourth switches are turned on.

5. The apparatus of claim 4, wherein the voltage generating circuit further comprises:

a clock signal generator configured to generate first, second and third clock signals;

a level shifter circuit configured to selectively change a level of the input voltage in response to the third clock signal to output a switching control signal; and wherein

the first and second switches are switched in response to first and second clock signals; and

the third and fourth switches are switched in response to a switch control signal.

6. The apparatus of claim 5, wherein

the third clock signal has an inverted phase with respect to the first clock signal;

a front edge of the second clock signal is delayed by a fixed time with respect to a front edge of the first clock signal; and

an active period of the second clock signal is narrower than that of the first clock signal.

7. The apparatus of claim 5, wherein the level shifter includes a metal-

oxide silicon (MOS) capacitor.

8. The apparatus of claim 5, wherein the switch control signal swings between the level of the input voltage and substantially double the level of the input voltage.

9. The apparatus of claim 8, wherein the fourth switch is turned on during a non-active status of the switching control signal, and the third switch is turned on during an active status of the switching control signal.

10. The apparatus of claim 1, wherein the control circuit is configured to generate the control current based on the boosted voltage and a desired boosted voltage.

11. The apparatus of claim 1, wherein the control circuit is configured to generate the control current based on a difference between the boosted voltage and the desired boosted voltage.

12. The apparatus of claim 1, wherein the control circuit comprises:

a voltage divider configured to generate a divided voltage from the boosted voltage;

a comparator configured to compare the divided voltage with a reference voltage; and

a current generator configured to generate the control current based on

output from the comparator.

13. The apparatus of claim 12, wherein the reference voltage represents a desired boosted voltage.

14. The apparatus of claim 1, wherein the control circuit comprises:

a voltage divider configured to divide the boosted voltage to generate a divided voltage;

an amplifier configured to amplify a difference voltage between a reference voltage and the divided voltage; and

a voltage controlled current source configured to generate the control current based on the amplified difference voltage.

15. The apparatus of claim 14, wherein the reference voltage represents a desired boosted voltage.

16. The apparatus of claim 14, wherein voltage controlled current source decreases the control current when the divided voltage is higher than the reference voltage, and increases the control current when the divided voltage is lower than the reference voltage.

17. A method for controlling a boosted voltage, comprising:

generating a boosted voltage from an input voltage based on a control current; and

generating the control current based on the boosted voltage.

18. The method of claim 17, wherein the generating a boosted voltage step comprises:

selectively storing charges corresponding to the input voltage in a capacitor; and

selectively outputting the stored charges in conjunction with charges corresponding to the control current as the boosted voltage.

19. The method of claim 18, wherein the generating the control current step generates the control current based on a difference between the boosted voltage and a desired boosted voltage.

20. The method of claim 17, wherein the generating the control current step generates the control current based on the boosted voltage and a desired boosted voltage.

21. The method of claim 20, wherein the generating the control current step generates the control current based on a difference between the boosted voltage and the desired boosted voltage.

22. The method of claim 17, wherein the generating the control current step comprises:

generating a divided voltage from the boosted voltage by dividing the

boosted voltage;

a comparing the divided voltage with a reference voltage; and

generating the control current based on output from the comparing step.

23. The method of claim 22, wherein the reference voltage represents a desired boosted voltage.

24. The method of claim 17, wherein the generating the control current step comprises:

dividing the boosted voltage to generate a divided voltage;

amplifying a difference voltage between a reference voltage and the divided voltage; and

generating the control current based on the amplified difference voltage.

25. The method of claim 24, wherein the reference voltage represents a desired boosted voltage.